

What is claimed is:

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1 1. A speed converter for converting the speed of packets
2 transmitted between first and second communication nodes respectively
3 attached to first and second IEEE-1394 serial buses, comprising:
4 a first transceiver node for receiving an inbound first packet at a
5 first speed from the first bus and transmitting an inbound second packet
6 as an outbound second packet at the first speed to the first bus;
7 a second transceiver node for transmitting said inbound first packet
8 as an outbound first packet at a second speed to the second bus and
9 receiving said inbound second packet at the second speed from the
10 second bus; and
11 header translation circuitry for translating destination identifier of
12 said inbound first packet to destination identifier of said outbound first
13 packet according to a mapped relationship between the first transceiver
14 node and the second communication node, and translating destination
15 identifier of said inbound second packet to destination identifier of said
16 outbound second packet.

1 2. The speed converter of claim 1, wherein the first transceiver
2 node comprises:
3 a first physical layer processor connected to said first bus;
4 a first link layer processor connected to the first physical layer
5 processor; and
6 first speed setting means for setting a value representative of said
7 first speed into said first link layer processor,
8 wherein said second transceiver node comprises:

9 a second physical layer processor connected to said second bus;
10 a second link layer processor connected to the second physical layer
11 processor; and
12 second speed setting means for setting a value representative of
13 said second speed into said second link layer processor,
14 wherein said header translation circuitry comprises:
15 a memory for storing identifiers for mapping said first transceiver
16 node to said second communication node; and
17 control circuitry connected to said first and second link layer
18 processors for receiving a packet therefrom and rewriting destination
19 identifier of the packet according to the identifiers stored in said
20 memory when a transaction is initiated from said first bus.

1 3. The speed converter of claim 1, wherein said memory further
2 stores identifiers for mapping said second transceiver node to said first
3 communication node, and wherein said control circuitry receives a
4 packet from said second transceiver node and rewrites destination
5 identifier of the packet according to the identifiers stored in said
6 memory when a transaction is initiated from said second bus.

1 4. A speed converter for converting the speed of packets
2 transmitted between a plurality of first communication nodes attached
3 to a first IEEE-1394 serial bus and a plurality of second communication
4 nodes attached to a second IEEE-1394 serial bus, comprising:
5 at least one first repeater node connected to the first bus;
6 a first transceiver node for receiving an inbound first asynchronous
7 packet from the first bus at a first speed via said at least one first

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8 repeater node and transmitting an inbound second asynchronous packet
9 as an outbound second asynchronous packet at the first speed to the first
10 bus via said at least one first repeater node, the first transceiver node
11 having identifiers identifying the first transceiver node itself and said at
12 least one first repeater node;

13 at least one second repeater node connected to the second bus;

14 a second transceiver node for transmitting said inbound first
15 asynchronous packet as an outbound first asynchronous packet to the
16 second bus at a second speed via at least one second repeater node and
17 receiving the inbound second asynchronous packet from the second bus
18 at the second speed via said at least one second repeater node and
19 receiving said inbound second asynchronous packet at the second speed
20 from the second bus via said at least one second repeater node, the
21 second transceiver node having identifiers identifying the second
22 transceiver node itself and said at least one second repeater node; and

23 header translation circuitry for translating destination identifier of
24 said inbound first asynchronous packet received by the first transceiver
25 node to destination identifier of said outbound first asynchronous
26 packet according to mapped relationships between said second
27 communication nodes and said first transceiver node and said at least
28 one first repeater node, and translating destination identifier of said
29 inbound second asynchronous packet received by the second transceiver
30 node to destination identifier of said outbound second asynchronous
31 packet according to mapped relationships between said first
32 communication nodes and said second transceiver node and said at
33 least one second repeater node.

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1 7 The speed converter of claim 4, wherein the first transceiver
2 node comprises:
3 a first physical layer processor;
4 a first link layer processor connected to the first physical layer
5 processor; and
6 first speed setting means for setting a value representative of said
7 first speed into said first link layer processor,
8 wherein said at least one first repeater node comprises a third
9 physical layer processor connected in series between said first bus and
10 said first physical processor;
11 wherein said second transceiver node comprises:
12 a fourth physical layer processor;
13 a second link layer processor connected to the fourth physical layer
14 processor; and

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8. The speed converter of claim 2 or 7, wherein said first link layer processor includes first register means for setting a first channel number and said second link layer processor includes second register means for setting a second channel number,

said second link layer processor receiving an isochronous packet containing said second channel number from said second bus at said second speed and forwarding the received packet to said first link layer processor via a data path,

said first link layer processor translating the channel number of said isochronous packet forwarded from said second link layer

11 processor to said first channel number and transmitting the channel
12 number translated isochronous packet toward the first bus at said first
13 speed.

1 9. The speed converter of claim 4,
2 wherein the first transceiver node is responsive to receipt of a first
3 asynchronous request packet requesting start or end of transmission of
4 isochronous packets from said first bus for forwarding the received first
5 asynchronous request packet to said second transceiver node,
6 wherein the second transceiver node is responsive to the first
7 asynchronous request packet from the first transceiver node for setting
8 the second transceiver node in a state for preparing start or end of
9 transmission of isochronous packets to said second bus,
10 wherein the first transceiver node is responsive to receipt of a
11 second asynchronous request packet requesting start or end of reception
12 of isochronous packets from said first bus for setting the first transceiver
13 node in a state for preparing start or end of transmission of isochronous
14 packets to the first bus.

1 10. The speed converter of claim 9,
2 wherein the second transceiver node transmits an asynchronous
3 request packet to the second bus requesting one of the communication
4 nodes on the second bus for starting or ending transmission of
5 isochronous packets when the first transceiver node receives said first
6 asynchronous request packet from the first bus,
7 wherein the second transceiver node transmits an asynchronous
8 request packet to the second bus requesting said one communication

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9 node to set in a state preparing for start or end of reception of
10 isochronous packets when the first transceiver node receives said
11 second asynchronous request packet from the first bus.

1 11. The speed converter of claim 10, wherein one of said first and
2 second transceiver nodes includes bus reset recovery means responsive
3 to an occurrence of a bus reset for resetting said one of the
4 communication nodes in the state which was attained when said bus
5 reset occurred.

1 12. The speed converter of claim 10, wherein said first transceiver
2 node includes an output master plug register (oMPR), an input master
3 plug register (iMPR), an output plug control register (oPCR) and an
4 input plug control register (iPCR), all of said plug and control registers
5 being specified according to IEC-61883 standard,
6 wherein said first transceiver node (211) is arranged to initialize
7 said plug and control registers according to values set in said one
8 communication node on said second bus, and modify values set in data
9 rate capability field of said oMPR and iMPR and a value set in data rate
10 field of said oPCR to said first speed.

1 13. The speed converter of claim 12,
2 wherein said first transceiver node translates a first channel
3 number contained in a first isochronous packet from said second bus to
4 a second channel number set in channel number field of said oPCR
5 when a value indicating transmission of an isochronous packet is set in
6 said oMPR,

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7 wherein said first transceiver node translates the second channel
8 number contained in a second isochronous packet from said first bus to
9 said first channel number contained in said first isochronous packet
10 when a value indicating reception of an isochronous packet is set in said
11 iPCR.

1 14. The speed converter of claim 13, wherein said first channel
2 number is a default number of decimal 63.

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1 15. The speed converter of any one of claims ^{7 and 9}4 to 14, wherein the
2 asynchronous packet received from one of said first and second buses is
3 a configuration ROM read request packet for accessing a configuration
4 ROM having a bus address in the range between a hexadecimal value of
5 FFFF F000 0400 and a hexadecimal value of FFFF F000 07FC.

1 16. The speed converter of any one of claims ^{7 and 9}4 to 14,
2 wherein said memory stores configuration ROM data of the
3 communication nodes of said first and second buses,
4 wherein said first transceiver node is responsive to receipt of a
5 configuration ROM read request packet from said first bus for reading
6 configuration ROM data from said memory corresponding to the
7 destination identifier contained in the received read request packet and
8 transmitting a read response packet to the first bus containing the read
9 configuration ROM data,
10 wherein said second transceiver node is responsive to receipt of a
11 configuration ROM read request packet from said second bus for
12 reading configuration ROM data from said memory corresponding to

13 the destination identifier contained in the received read request packet
14 and transmitting a read response packet to the second bus containing
15 the read configuration ROM data.

1 17. The speed converter of claim 16, wherein the configuration
2 ROM data stored in said memory by rewriting lower 64 bits of
3 Bus_Info_Block of configuration ROM data of each of said
4 communication nodes and lower 64 bits of Node_Unique_Id leaf with
5 64-bit Extended Unique Identifier and rewriting module_vendor_id
6 field of Module_Vendor_Id entry with a company ID indicating the
7 manufacturer of the speed converter.

1 18. A speed converter for converting the speed of packets
2 transmitted between a plurality of first communication nodes attached
3 respectively to a plurality of first IEEE-1394 serial buses and at least one
4 second communication node attached to a second bus, comprising:

5 a plurality of speed conversion units associated respectively with
6 said plurality of first buses, each of said speed conversion units
7 including:

8 a first transceiver node for receiving an inbound first packet at a
9 first speed from the associated first bus and transmitting an inbound
10 second packet as an outbound second packet at the first speed to the
11 associated first bus;

12 a second transceiver node for transmitting said inbound first packet
13 as an outbound first packet at a second speed to the second bus and
14 receiving said inbound second packet at the second speed from the
15 second bus; and

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16 header translation circuitry for translating destination identifier of
17 said inbound first packet to destination identifier of said outbound first
18 packet according to mapped relationship between the first
19 communication node of the associated first bus and said at least one
20 second communication node, and translating destination identifier of
21 said inbound second packet to destination identifier of said outbound
22 second packet.

1 19. A method of converting the transmission speed of packets
2 transmitted between a first communication node and a second
3 communication node respectively attached to first and second IEEE-
4 1394 serial buses, comprising:
5 receiving, at a first transceiver node, an inbound first packet
6 transmitted at a first speed from said first bus;
7 translating destination identifier of said inbound first packet to
8 destination identifier of an outbound first packet;
9 transmitting the outbound first packet from a second transceiver
10 node to the second bus at a second speed;
11 receiving, at said second transceiver node, an inbound second
12 packet at said second speed from said second bus;
13 translating destination identifier of said inbound second packet to
14 destination identifier of an outbound second packet; and
15 transmitting the outbound second packet from the first transceiver
16 node to said first bus at said first speed.

1 20. The method of claim 19, further comprising:

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2 setting a first channel number in said first transceiver node and
3 setting a second channel number in said second transceiver node;
4 receiving, at said second transceiver node, an isochronous packet
5 containing a second channel number from said second bus at said
6 second speed;
7 translating the channel number of said isochronous packet to said
8 first channel number at said first transceiver node; and
9 transmitting the channel-translated isochronous packet from the
10 first transceiver node to the first bus at said first speed.

1 21. A method of converting the speed of packets transmitted
2 between a plurality of first communication nodes attached to a first
3 IEEE-1394 serial bus and a plurality of second communication nodes
4 attached to a second IEEE-1394 serial bus, comprising:
5 receiving, at a first transceiver node, an inbound first packet from
6 the first bus at a first speed via at least one first repeater node;
7 translating destination identifier of said inbound first packet to
8 destination identifier of an outbound first packet according to
9 relationships between said second communication nodes and said first
10 transceiver node and said at least one first repeater node;
11 transmitting from a second transceiver node said outbound first
12 packet to the second bus at a second speed via at least one second
13 repeater node;
14 receiving, at said second transceiver node, an inbound second
15 packet from the second bus at the second speed via said at least one
16 second repeater node;

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17 translating destination identifier of said inbound second packet to
18 destination identifier of an outbound second packet according to
19 relationships between said first communication nodes and said second
20 transceiver node and said at least one second repeater node; and
21 transmitting from the first transceiver node said outbound second
22 packet to the first bus via said at least one first repeater node at said first
23 speed.

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